IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Srinivasan (nmi) Chakravarthi et al.
Serial No.:	To be Determined
Filing Date:	December 1, 2003
Group Art Unit:	Unassigned
Examiner:	Unassigned
Title:	*Forming a Retrograde Well in a Transistor to Enhance Performance of the Transistor*

MAIL STOP: PATENT APPLICATION
Commissioner For Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Attorney Docket No. TI-36386 (032350.B538)
Express Mail Certificate No. **EV 323507496 US**

Dear Sir:

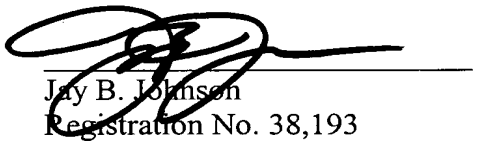
INFORMATION DISCLOSURE STATEMENT

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97, and 1.98, that the documents listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), Applicants makes no representation that these documents qualify as prior art or that these documents are material to patentability of the present application or that a search has been made.

Since the present Application was filed after June 30, 2003, a copy of any U.S. Patent and any U.S. Patent Application Publication cited on the attached PTO Form 1449 is not being submitted with this Information Disclosure Statement pursuant to the July 11, 2003 waiver of 37 C.F.R. S 1.98(a)(2)(i) by the U.S. Patent and Trademark Office.

Respectfully submitted,

BAKER BOTTS L.L.P.
Attorneys for Applicants



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Date: December 1, 2003

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Customer Number: **23494**

PTO-1449	Application No.	Applicant(s)
Information Disclosure Citation In an Application	**To be Assigned**	**Srinivasan (nmi) Chakravarthi et al.**
	Docket Number: **TI-36386 (032350.B538)**	Group Art Unit: **To be Assigned**
		Filing Date: **December 1, 2003**

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

NON-PATENT DOCUMENTS

		NONPATENT DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	A	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Abstract," Intel Technologies Journal, 3rd Quarter 1998, pp. 1-2	September 1998
	B	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Oxide Scaling,," Intel Technologies Journal, 3rd Quarter 1998, pp. 1-9	September 1998
	C	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Source Drain Engineering," Intel Technologies Journal, 3rd Quarter 1998, pp. 1-10	September 1998
	D	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Channel Engineering, " Intel Technologies Journal, 3rd Quarter 1998, pp. 1-11	September 1998
	E	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Circuit and Device Interactions, " Intel Technologies Journal, 3rd Quarter 1998, pp. 1-6	September 1998
	F	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Alternate Device Options, " Intel Technologies Journal, 3rd Quarter 1998, pp. 1-6	September 1998
	G	Scott Thompson, "MOS Scaling: Transistor Challenges for the 21st Century – Conclusion, " Intel Technologies Journal, 3rd Quarter 1998, pp. 1	September 1998

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

U.S. PATENT AND TRADEMARK OFFICE